Timers and Counters.

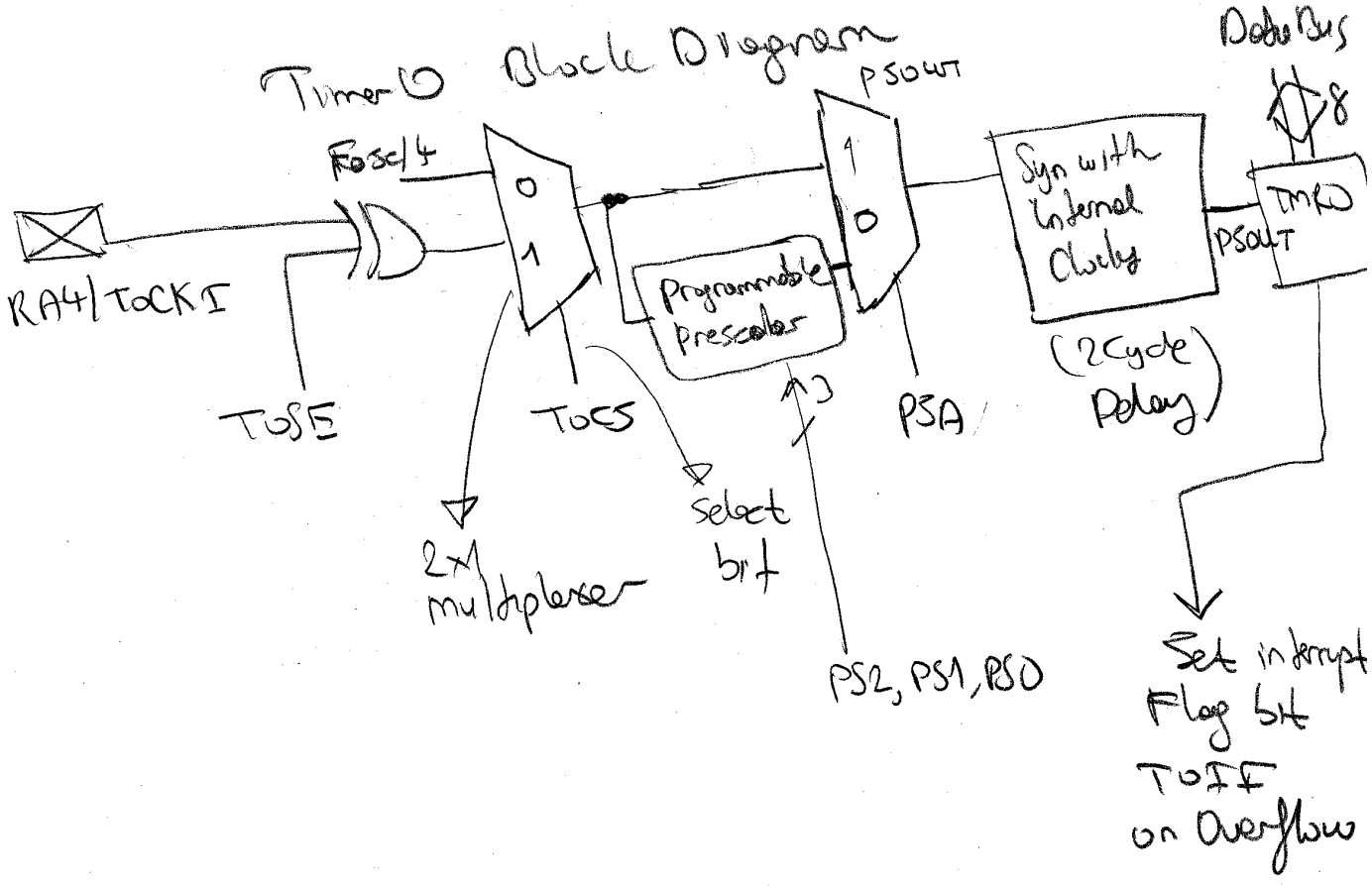
TMR0 → An 8-bit register

Functions of Timer & Counter

Timer0 module timer/counter has the following features

- 8-bit Timer-Counter
- Readable and writable
- Internal and external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt-on-overflow from 0xFF to 0x00

Timer0 Block Diagram



(2) OPTION REG

7	6	5	4	3	2	1	0
		T0CS	T0SE	PSA	PS2	PS1	PS0

T0CS: TMR0 Clock Source Select bit

1 = Transition on RA4/T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

T0SE: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on RA4/T0CKI pin

0 = Increment on low-to-high transition on RA4/T0CKI pin

PSA: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

PS2:PS0 Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

(3)

Timer mode is selected by clearing bit TOCS.
In timer mode TMR0 will increment every instruction cycle (without prescaler). If prescaler is set to a value, for instance, 64 then TMR0 will increment every 64 cycle.

Counter mode is selected by setting bit TOCS.
In this case Timer0 will increment either on every rising or falling edge on pin RA4/T0CKI.
The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE of the OPTION REG.

Prescaler: Prescaler is used to slow down the count operation

Ex: bcf OPTION_REG, T0CS → Timer Clock Source

↓ internal clock is selected for counting operation. i.e, at every clock counter is incremented

bsf OPTION_REG, T0CS

↓ External Clock on RA4/T0CKI is selected for counting clock

(4) Example:

bcf OPTION_REG, T0CS; → internal clock is selected

bcf OPTION_REG, PSA; → Prescaler is assigned to Timer0 module

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bsf OPTION_REG, PS0
bsf OPTION_REG, PS1
bsf OPTION_REG, PS2
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} PS2 PS1 PS0 = 111

↓ from table TMR0 Rate is 1:256

It means that at every 256 cycle Timer0 Counter increments

For 4mHz oscillator

1 Cycle is 1 µsec

After a full count 0 → 255 → 0 (256 count)

T0IF is set if Timer Interrupt is Enable

The time required for a full count for PS2 PS1 PS0 = 111

is 256 × 256 µsec

= 65536 µsec

= 65.5 msec ≃ 0.065 sec

(5) Timer0 Interrupts

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. The overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut-off during SLEEP.

Notes: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

- Timer starts counting when you write something to Timer0 register.