(1) Ex:

For 4mHz oscillator

Prescaler Value K = 2, 4, 8, 16, 32, 64, 128, 256 can be

If Timer Register Contains Integer N initially

Interrupt signal is generated and TOIF Flag is set after

$T = (256 - N) \cdot K$ τ_{sec}

1 cycle For 4mHz Oscillator

Ex:

Initialize Timer Register Such that Interrupt (Timer) occurs every 1msec.

Sln:

$(256 - N) \cdot K = 1000$

There are some parameter values satisfying above equation

$(256 - N)K = 1000$

$N = 0$ OR $N = 125$

$K = 4$ $K = 8$

(2) Ex:

At each turn of a full count (Timer Register) PORTB value is incremented.
Use Time Interrupt Facility

Sln:

```
list p=16f84A
include "p16f84A.INC"
 org  0x000;
 goto main
  org 0x004;
   goto increment_PORTB;

main  bsf STATUS, RP0;
      clrf TRISB;
      movlw b'00000111';
      movwf OPTION_REG;
      bcf STATUS, RP0;
      clrf TMR0; ⟶ timer starts counting
       bsf INTCON, GIE
        bsf INTCON, T0IE;
        bcf INTCON, T0IF;
         clrf PORTB;
increment_PORTB;
        bcf INTCON, T0IF;
         incf PORTB, F;
          clrf TMR0;
           retfie;
          end
```

clears time and prescaler value

(3) Watchdog Timer (WDT)

The watchdog timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction.

- During normal operation, a WDT time-out generates a device RESET.

WDT Periods

The WDT has a nominal time-out period of 18 ms (with no prescaler).

If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION-REG register.

- Thus, time-out periods up to 2.3 seconds can be realized.
- The $\overline{TO}$ bit in STATUS register will be cleared upon a WDT time-out.