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DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation.

The following registers are used to read and write EEPROM memory.

EECON1

EECON2 → (not a physically implemented register)

EEDATA

EEADR

EEDATA → holds the 8-bit data for read/write

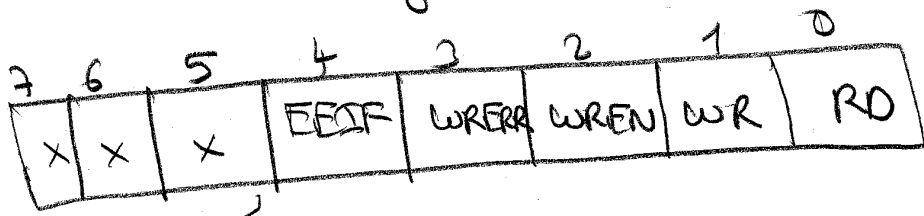
EEADR → holds the address of EEPROM location being accessed.

EECON1 } used to control read/write operation

EECON2

EECON2 → is used when writing something to EEPROM

EECON1 Register (located at 0x88h)



not implemented

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EEIF \rightarrow EEPROM Write Operation Interrupt Flag bit

1 = The write operation is completed (must be cleared in software)

0 = The write operation is not complete or has not been started

WRERR \rightarrow EEPROM Error Flag bit

1 = A write operation is not successful

0 = The write operation is completed

WREN \rightarrow EEPROM Write Enable bit

1 = Allow write cycles

0 = Inhibits write to the EEPROM

WR \rightarrow Write Control bit

1 = Starts writing operation. The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software

0 = Write cycle to the EEPROM is complete

RD \rightarrow Read Control bit

1 = Starts an EEPROM read. The RD bit can only be set (not cleared) in software

0 = Does not initiate an EEPROM read

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Ex 3

Reading the EEPROM Data Memory

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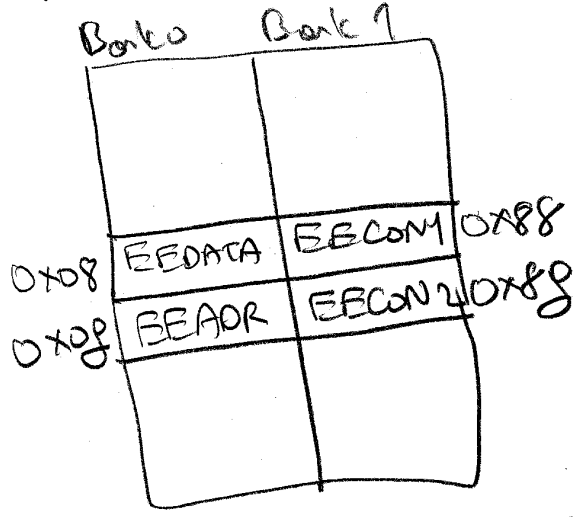
bcf STATUS, RPO; Bank 0
movlw CONFIG-ADDR;
movwf EEADR; Address to read
bsf STATUS, RPO; Bank 1
bsf EECOML, RD; EE Read starts
bcf STATUS, RPO; Bank 0
movf EEData, W; W = EEData

```

Write address to EEADR

set RD bit of EECOML

read data is in EEData register



Writing to the EEPROM Data Memory

Ex 3

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEData register. Then the user must follow a specific sequence to initiate the write for each byte.

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write 0x00
movlw CONFIG-ADDR;
movwf EEADR,
movlw .10,
movwf EEEDATA;
bsf STATUS,RP0; Bank 1
bcf INTCN, GIE; Disable INTs
bsf EECON1, WREN; Enable write

A

movlw 0x55;
movwf EECON2,
movlw 0xAA;
movwf EECON2;
bsf EECON1, WR; set WR bit, begin
write
bsf INTCN, GIE; Enable INTs

Required sequence for every write operation

Ex 3

Slm

write 20 to EEPROM location 0x03

movlw 0x03,
movwf EEADR,
movlw .20,
movwf EEEDATA
bsf STATUS,RP0,
bcf INTCN, GIE
bsf EECON1, WREN

A → required sequence